

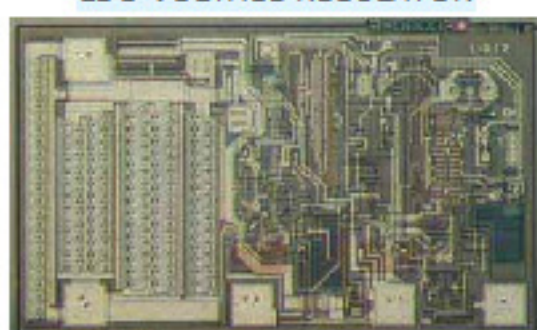
FEATURES

Input/Output Typ. 0.4V
400mA Output Current
Low Quiescent Current
Reverse Polarity Protection
Over Voltage Protection ($\pm 60V$)
Foldback Current Limiting
Thermal Shutdown

APPLICATIONS

In DIE form, this device is an excellent selection for many chip and wire HYBRID CIRCUITS

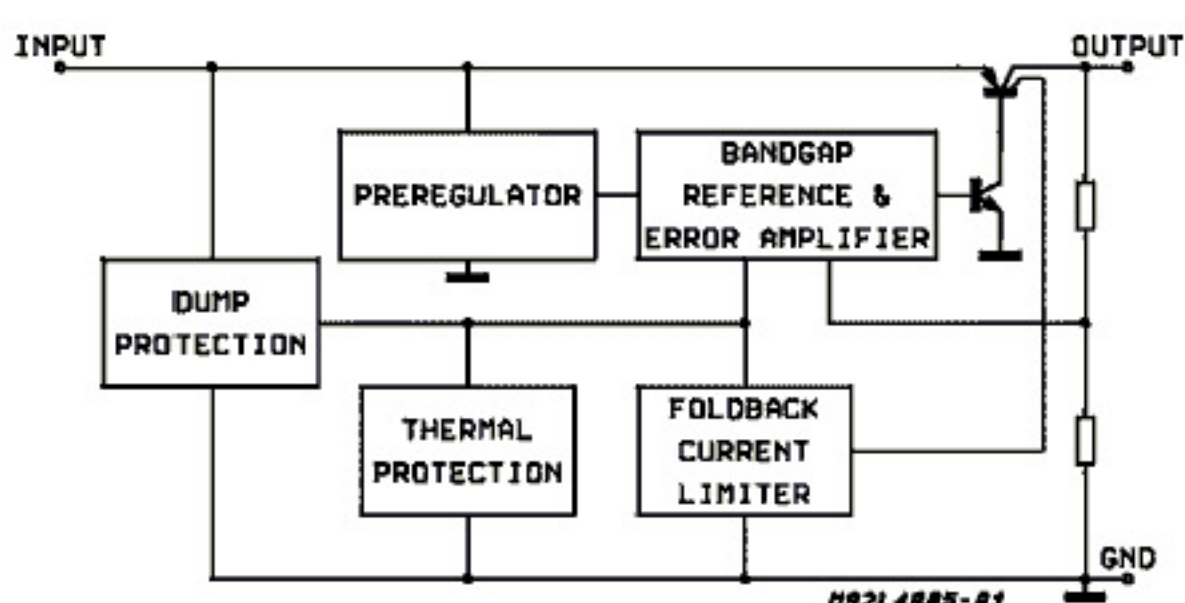
LDO VOLTAGE REGULATOR



PRODUCT DESCRIPTION AND SHORT APPLICATION NOTE

The USM L4812 series devices are voltage regulator with a very low voltage drop (typically 0.4 V at fullrated current), output current up to 400mA, low current and comprehensive on-chip protection. The-quiescentse devices are protected against load dump and field decay transients of $\pm 60V$, polarity reversal and overheating. A foldback current limiter protects against load short circuits. Available in 5V, 8.5V 9.2V, 10V and 12V versions (all $\pm 4%$, $T_I = 25^\circ C$) the-quiescentse regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.

IC SCHEMATIC DIAGRAM



MAXIMUM RATINGS

PARAMETER	VALUE	UNITS
DC Input Voltage	+35	V
DC Input Reverse Voltage	-18	V
Transient Input Overvoltages		
LoadDump:	60	V
5ms =< Trise =< 10ms, tf Fall Time Constant = 100ms, Rsource =< 0.5		
FieldDecay:	-60	V
5ms =< Tfall =< 10ms, Rsource =< 10		
tr Rise Time Constant = 33ms		
Junction and Storage Temperature Range	-55 to +150	$^\circ C$

ONLY Proper die handling equipment and procedures should be employed. Stresses beyond listed absolute maximum ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTIC

$V_I=14.4V; C_O=100F; T_J=25^\circ C$ unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	LIMIT	UNITS
Output Voltage	V_O	$I_O=5mA$ to 400mA	8.83	9.20	9.57	V
Operating Input Voltage	V_I				26	V
Line Regulation	DV_O/V_O	$V_I=13$ to 26V; $I_O=5mA$		1	10	mV/V
Load Regulation	DV_O/V_O	$I_O= 5$ to 400mA*		3	15	mV/V
Dropout Voltage	V_I-V_O	$I_L = 150mA$ $I_L = 400mA^*$		0.2 0.4	0.4 0.7	V
QuiescentCurrent	I_q	$I_L = 0mA$ $I_L = 150mA$ $I_L = 400mA^*$		0.8 25 65	2 45 90	mA
Temperature Output Voltage Drift	DV_O/DT^*V_O			0.1		mV/ $^\circ C^*V$
Supply Voltage Rejection	S_{VR}	$I_O=350mA; f=320Hz;$ $C_O=100F; V_I=V_O+3V+2V_{pp}$		60		dB
Maximum Output Current	I_O			800		mA
Output Short Circuit Current (fold back condition)	I_{SC}			350	500	mA

ELECTRICAL CHARACTERISTIC

$V_I=14.4V; C_O=100F; T_J=-40$ to $125^\circ C$ (note1) unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	LIMIT	UNITS
Output Voltage	V_O	$I_O=5mA$ to 400mA	8.65	9.20	9.75	V
Operating Input Voltage	V_I	Note 2			26	V
Line Regulation	DV_O/V_O	$V_I=13$ to 26V; $I_O=5mA$		2	15	mV/V
Load Regulation	DV_O/V_O	$I_O=5$ to 400mA*		5	25	mV/V
Dropout Voltage	V_I-V_O	$I_L = 150mA$ $I_L = 400mA^*$		0.25 0.5	0.5 0.9	V
QuiescentCurrent	I_q	$I_L = 0mA$ $I_L = 150mA$ $I_L = 400mA^*$		1.2 40 80	3 70 140	mA
Maximum Output Current	I_O			870		mA
Output Short Circuit Current (fold back condition)	I_{SC}			230		mA

(NOTE 1) This limits are guaranteed by design, correlation and statistical control on production samples over the indicated temperature and supply voltage ranges.

(NOTE 2) For a DC voltage 26V < 35V the device is not operating.

GENERAL DIE INFORMATION

Substrate	Thickness (mils)	Die size (mils) [mm]	Bonding pads	Backside metal
Silicon	10 \pm 1	(101.181x61.811) [2.57x1.57]	min 7x7 mils, 1 μm thick, aluminium	Backside of the die is coated with 0.5 μm GOLD , which makes it compatible with AuSi or AuGe die attach.

All US Microwaves products are available in die form. Typical delivery for die products is 2-3 weeks ARO. For Custom designs, delivery is 3-4 weeks ARO. Certain items may be available from stock. Inventory is periodically updated. All devices for chip and wire applications are 100% tested, visual inspected and shipped in waffle packs (WP). For high volume automated assembly, MIS chip capacitors are supplied as 4" wafers 100% tested, inked and diced on expanded film frame (FF).

TECHNOLOGY DESCRIPTION: SEMICONDUCTOR-MANUFACTURING

These integrated Circuits are manufactured with medium voltage junction isolated bipolar process. junction isolated bipolar processes allow integration of high performance NPN, PNP and JFET transistors, MOS capacitors, diffused resistors and precision thin film resistors. The bond pad metallization is standard 1 μm Aluminium. The backside of the die is coated with 0.5 μm GOLD , which makes it compatible with AuSi or AuGe die attach.

All US Microwaves products are manufactured using GOLDCHIP TECHNOLOGY™ a trade mark of Semiconix Corporation.

DIE LAYOUT - MECHANICAL SPECIFICATIONS

PAD #	FUNCTION	X(mils)	X(mm)	Y(mils)	Y(mm)
1	INPUT	10.827	0.275	50.394	1.280
2	OUTPUT	10.827	0.275	3.543	0.090
3	OUTPUT	42.520	1.080	3.543	0.090
4	GND	69.488	1.765	3.543	0.090
5	SHUTDOWN	90.354	2.295	3.543	0.090

